[MULTILAYER SILICON OVER INSULATOR DEVICE]

DESCRIPTION

Background of Invention

[Para 1] Field of the Invention

[Para 2] The invention relates to stacked circuits, and more particularly to stacked circuits having different crystal orientations.

[Para 3] Background Description

[Para 4] SOI (silicon over insulator) technology eliminates bulk CMOS latch-up. SOI technology additionally reduces junction capacitance and allows circuits to operate at higher speeds. Accordingly, SOI technology allows a higher circuit density to be achieved on a silicon wafer.

[Para 5] SOI technology can be applied to many levels of devices. Each level of a multilevel SOI technology based device may be interconnected using vertical plugs which additionally allows metal connections to be used at any level. In a multilevel device, NMOS and PMOS devices may each be restricted to a separate level, or NMOS and PMOS devices may be intermixed on a single level.

[Para 6] For some types of semiconductor devices, it is advantageous to have multiple layers of similar semiconductor material, where each layer has a crystal orientation different from the adjoining layers. However, multi-layer devices are formed with similar semiconductor material having the same crystal orientation from one level to the next. This limitation imposed on the crystal orientation across multiple levels of an integrated circuit results from constraints imposed by the fabrication process.

[Para 7] In particular, semiconductor material is traditionally grown from a pre-existing layer of semiconductor material. During the material growth process, the atoms of the newly formed layer have a strong tendency to orient themselves to the pre-existing substrate's crystal structure as they are laid down. Thus, it becomes very difficult to create a new layer of similar semiconductor material having a crystal orientation which is different from the underlying layer.

Summary of Invention

[Para 8] In a first aspect of the invention, a method of forming a circuit includes forming a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation, and forming an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation. The method also includes superimposing the upper semiconductor device on the lower semiconductor device.

[Para 9] In another aspect of the invention, a method of forming an inverter includes forming a lower semiconductor layer comprising a first crystal orientation, and forming at least one lower source/drain region in the lower semiconductor layer. The method also includes forming a lower gate on the lower semiconductor layer to define an active region in the lower semiconductor layer, and forming an upper semiconductor layer comprising a second crystal orientation. The method additionally includes forming at least one upper source/drain region in the upper semiconductor layer, and forming an upper gate on the upper semiconductor layer to define an active region in the upper semiconductor layer. The method further includes bonding the upper semiconductor layer to the lower semiconductor layer, and electrically connecting the at least one lower source/drain region to the at least one upper source/drain region.

[Para 10] In another aspect of the invention, a circuit includes a lower semiconductor device having an active region comprising a semiconductor

with a first crystal orientation, and an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor device is superimposed on the lower semiconductor device.

Brief Description of Drawings

[Para 11] Figure 1 illustrates an embodiment of a multilayer device in accordance with the invention; and

[Para 12] Figures 2 -7 illustrates steps in fabricating a multilayer device in accordance with the invention.

Detailed Description

[Para 13] In embodiments of the invention, a first CMOS device, such as a pFET, is formed having a first crystal orientation in the active region of the device, and a second CMOS device, such as an nFET, is formed having a second orientation in the active region of the second device. After both devices are formed, the second device is bonded to the first device with a bonding layer such as SiO_2 forming a stacked or layered arrangement. Once the two devices are bonded in the stacked arrangement, the devices are interconnected with conductive pathways such as tungsten plugs and/or metal interconnects. Thus, it is possible to form stacked layers of CMOS devices where each layer has either the same or a different crystal orientation in the active region as a layer below it and/or a layer above it.

[Para 14] Referring to Figure 1, an embodiment of a multilayer device in accordance with the invention is shown. Figure 1 may equally represent a fabrication process. The multilayer device 100 includes a first device 50, for example, a pFET, onto which a second device 52, for example, an nFET, is bonded. The first device 50 and the second device 52 each have a different crystal orientation from one another in the active region of the multilayer device 100.

[Para 15] In more detail, the first device 50 has Si substrate 10 with a crystal orientation of [100] and a SiO_2 layer 12 is formed on top of the silicon (Si) substrate 10. On top of the SiO_2 layer 12, a Si layer 14 is formed having a crystal orientation of [100]. Trenches are etched and filled with an insulating material such as an oxide to form shallow trench isolations 18 on either side of the active region of the first Si layer 14. Source/drain regions 16 are formed next to shallow trench isolations 18 in the first Si layer 14. The source/drain regions 16 are formed by any of the methods well known in the art for forming source/drain regions.

[Para 16] The upper surface of the first Si layer 14 is planarized after the source/drain regions 16 are formed using any of the methods well known in the art to planarize a Si layer. A second SiO_2 layer 20 is formed on the top surface of the first Si layer 14. A first gate 26 is then formed within the second SiO_2layer 20 such that a portion of the first SiO2layer 20 forms a gate oxide for the first gate 26 of the first device 50.

[Para 17] In addition to the first device 50 being formed, the second device 52 is also formed using similar fabrication methods appropriate for producing the second device 52. However, the second device 52 has a crystal orientation in its active region different from the first device 50. This is possible due to the separate fabrication processes of each of the devices, prior to bonding. Accordingly, a second Si layer 30 having a crystal orientation of [110] is formed to be the active region of the second device 52. Trenches are etched into the second Si layer 30 and filled with an insulator such as an oxide using any of the methods well known in the art for forming and filling a trench to create second shallow trench isolations 34. Source/drain regions 32 are formed next to the shallow trench isolations 34. The source/drain regions 32 of the second device 52 are formed by any of the methods well known in the art for forming source/drain regions 32 of the second device 52.

[Para 18] After the source/drain regions 32 are formed in the second device 52, a gate oxide 35 is formed on top of the active region of the second Si layer 30. The gate oxide 35 may be formed by any of the techniques well known in

the art for forming a gate oxide. After the gate oxide 35 is formed, a gate 36 is formed on top of the gate oxide 35, thus completing the formation of the second device 52.

[Para 19] Once the poly gate 36 of the second device 52 is formed, metal contacts to the various inputs of the second device 52 are formed. For example, a first and second metal 38 are formed in contact with the source/drain regions 32 of the second device. Additionally, a lower poly contact 42 to voltage bus 46 is formed in contact with the poly gate 36.

[Para 20] Once the first device 50 and the second device 52 are formed, the second device 52 is bonded to the top of the first device 50 with a bonding layer 15. The bonding layer 15 attaches a top of the first device 50 to a bottom of the second device 52 and attaches to a Si layer 27 with a crystal orientation of [110] formed on a bottom of the second device 52. The bonding layer 15 bonds the upper device 52 to the lower device 50 using methods and materials well known in the art for bonding one device to another. The bonding layer 15 may include any insulating substance capable of bonding a first semiconductor device to a second semiconductor device, such as, for example, nanocleave method.

[Para 21] After the first device 50 and the second device 52 are bonded to one another, metal plugs are formed between the various metal connections of the first and second devices, 50 and 52. The source/drain of the upper and lower devices are connected to a metal plug 48 or V_0, and the source/drain of the upper device is connected to voltage bus 40, such as for example, V_{dd}. Similarly the source/drain of the lower device is connected to V_{ss} 24. Both gates are connected through a metal plug 46 or V_{in}.

[Para 22] The metal 38 is connected to the device through metal connect 41 MC and CA connect 39. Similarly, metal 2 44 is connected to the device through MC connect 45, and CA connects 25 and 47, and viaone 49, respectively.

[Para 23] In operation, the multilayer device of Figure 1, where the first device 50 is a pFET and the second device 52 is an nFET, is configured to function as a CMOS inverter. The CMOS inverter is configured to occupy half the surface area on the chip due to its multilayer structure. Additionally, the first and second devices, 50 and 52, of the CMOS device 100 are internally connected to one another, as discussed above, thereby simplifying the input and output leads to the CMOS device 100. It should be noted that the voltage buses, 24 and 40, may be laid out horizontally or vertically, due to the multilayer structure of the devices, 50 and 52. Also, in this manner, since the devices 50 and 52 are formed separately, it is now possible to obtain a stacked structure with different crystal orientations in the active region.

[Para 24] Referring to Figures 2-7, a method of forming an SOI island to form an active region of an embodiment of the invention is shown. Referring to Figure 2, a silicon wafer Si substrate 102 is shown. On top of the Si substrate 102, a thick oxide layer 104 is grown. The thick oxide layer 104 can be grown using any of the methods well known in the art for growing oxide layers such as dry or wet oxidation methods.Referring to Figure 3, a photoresist is deposited, imaged and patterned on top of the thick oxide 104. Next, the photoresist is used as a mask to etch islands 106 in the thick oxide layer 104. The islands 106 are etched down to the bottom of the thick oxide layer 104 and do not penetrate into the Si substrate 102.

[Para 25] Referring to Figure 4, a thin oxide 108 is formed at the bottom of the islands 106 on top of the Si wafer 102. The thin oxide 108 may be formed by any of the methods well know in the art to form a thin oxide layer in the bottom of a trench. Additionally, a seed hole 110 is opened from top to bottom of the thick oxide layer 104. Accordingly, the seed hole 110 passes through the thick oxide layer 104 and terminates at the Si substrate 102 allowing access to the Si substrate 102 from the top of the structure. The seed hole 110 was formed between the islands 106 using suitable etch methods known in the art such as plasma etching.

[Para 26] Referring to Figure 5, an epitaxial lateral overgrowth ("ELO") growing method is used to grow silicon starting at the bottom of the seed hole 110 on top of the exposed Si substrate 102. The ELO layer grows up and out of the seed hole 110 and over the top of the thick oxide 104 and down into the islands 106 to fill the islands 106 with silicon. Thus, a Si layer 112 is formed within a top of the islands 106, within the seed hole 110, over the top of the thick oxide 104. Because the Si layer 112 is grown starting at the top of the Si substrate 102, the crystal orientation of the silicon in the Si layer 112 is the same as the crystal orientation of the silicon in the Si substrate 102.

[Para 27] Referring to Figure 6,. After the Si layer 112 is formed, chemical mechanical polishing ("CMP") is used to remove the Si 112 which protrudes above the top surface of the thick oxide 104. Consequently, the thick oxide 104 is used as a local polish stop while the structure is planarized to isolate the silicon in the islands 106. Accordingly, the silicon of the Si layer 112 is left remaining in the islands 106 to form SOI islands 114. The SOI islands 114 are isolated from the silicon within the seed hole 110.

[Para 28] As mentioned above, because the Si layer 112 is grown while the seed is in contact with the Si substrate 102, the resulting Si layer 112 will have the same crystal orientation as the Si substrate 102. Furthermore, because the SOI islands 114 are formed from the Si layer 112, the SOI islands 114 will have the same crystal orientation as the Si substrate 102.

[Para 29] After the SOI islands 114 are formed, standard PMOS or NMOS processes may be utilized to form either a PMOS or NMOS device including forming source/drain regions, gate structures and metal contacts. Where the SOI islands 114 will form a PMOS device which will function as a first layer of a multilayer SOI device, a thick oxide layer will be formed on top of the PMOS device. Once a first layer PMOS device and a second layer NMOS device are formed, the NMOS device is bonded on top of the PMOS device forming the multilayer SOI device. It should be noted that the SOI islands of the NMOS device are grown with a crystal orientation of [100] and PMOS has an orientation of [110].

[Para 30] For example, referring to Figure 7, a first layer device 120 is bonded to a second layer device 118 with a thick oxide layer 122. Once the first layer 120 and second layer 118 are bonded to one another, the structure is etched to form viaplug holes. After the via plug holes are etched, a low temperature chemical vapor deposition ("CVD") process is used to fill the via plugs with tungsten forming tungsten plugs 126. Once the tungsten plugs 126 have been formed, CMP is used to planarize the tungsten plugs 126 and final passivation is performed. Although the example shows a two layer device for illustration purposes, the method may be extended to produce any desired number of layers with each layer having practically any desired crystal orientation.

[Para 31] Advantages of the multilayer SOI device include a reduction of about 50% of the area needed to create a circuit and using different crystal orientations for different devices. Additionally, where multilayer devices are symmetrical, the mask may be shared.

[Para 32] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.